IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In the Application of:	)
Pai	) Electronically Filed
	)
U.S. Serial No.: 10/736,125	) April 4, 2011
	)
Filed: 12/15/2003	)
	)
Examiner: Tseng	)
	)
Group Art Unit: 2184	)
	)
Confirmation No. 3609	)

REPLY BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Sir:

This is an appeal from the Office Action made Final mailed
April 12, 2010 in which claims 18-30 were rejected. A
Notice of Appeal was filed on August 12, 2010.

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I.   REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California and having a place of business at 16215 Alton Parkway, Irvine California 92618-3616, has acquired the entire right, title, and interest in and to the invention, the application, and any and all patents to be obtained therefore.

II.   RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III.   STATUS OF THE CLAIMS

Claims 1-17 are cancelled without prejudice.

Claims 18-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee.

Claims 18-30 are appealed

IV.   STATUS OF AMENDMENTS

There are no amendments pending in the present application.

V.   SUMMARY OF CLAIMED SUBJECT MATTER

Claim 18 is directed to a direct memory access controller, said direct memory access controller comprising (*Specification* at 12, Lines 18-19, Figure 4, DMA Engine 510):

a state logic machine for receiving a single command to provide a specified range of a plurality of

sequential data words, wherein the single command expressly states a starting address and an ending address of said specified range (*Specification* at 12, Lines 23-29, Figure 4, 605); and

a memory controller (*Specification* at 12, Line 19, Figure 4, 620) for fetching a first portion of the specified selectable range (*Specification* at 13, Lines 6-9) and a second portion of the specified selectable range after fetching the first portion, wherein the second portion of the range has a lower address than the first portion (*Specification* at 13, Lines 18-20), after the state logic receives the single command including the starting address and the ending address.

Claim 24 is directed to a method for fetching data words, said method comprising:

receiving a single command to provide a range of a plurality of sequential data words in a memory, wherein the command expressly states a starting at a beginning address and ending at an ending address of said range (*Specification* at 14, Lines 17-22);

fetching a portion, in a forward address order, of the range of sequential data words, said wherein said portion of the range of sequential data words consists of a predetermined amount of data words that conclude with and precede the ending address, and wherein the predetermined amount of data words is equivalent to a capacity of a local buffer (*Specification* at 15, Lines 6-8);

storing the predetermined amount of data words that conclude with and precede the ending address in the local buffer (*Specification* at 15, Lines 9-10);

fetching, in the forward address order, at least one preceding portion of the range of sequential data

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words, wherein each of the preceding portions of the range of sequential data words consist of the predetermined amount of data words (*Specification* 13, Lines 19-23); and

wherein a one of the preceding portions of the range of sequential data words comprises the starting address, truncating those data words that precede the beginning address (*Specification* at 14, Lines 28-32).

Claim 30 is directed to a system for decoding video data, said system comprising:

a memory for storing a packetized elementary stream, said packetized element stream comprising a plurality of packets (Figure 3, 505);

a start code table for storing starting addresses and ending addresses of said plurality of packets (Figure 3, 507);

a video decoder for decoding a particular one of the plurality of packets, wherein the video decoder looks up the starting addresses and the ending addresses of the particular one of the plurality of packets and issues a single command to fetch the packet, wherein the single command expressly includes a starting address and an ending address associated with the particular one of the plurality packets (Figure 2, 445); and

a direct memory access controller, said direct memory access controller comprising (*Specification* at 12, Lines 18-19, Figure 4, DMA Engine 510):

a state logic machine for receiving the single command (*Specification* at 12, Lines 23-29, Figure 4, 605); and

a memory controller (*Specification* at 12, Line 19, Figure 4, 620) for fetching a first portion of a range, said range comprising sequential data words from the

starting address to the ending address for the particular one of the plurality of packets (*Specification* at 13, Lines 6-9), and a second portion of the range after fetching the first portion, wherein the second portion of the range has a lower address than the first portion (*Specification* at 13, Lines 18-20), after the state logic receives the single command including the starting address and the ending address.

VI.   GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Rejection of claims 18-30 under 35 U.S.C. 102(e) as anticipated by Lee (U.S. Patent No. 6,842,219).

VII. ARGUMENT: CLAIM 18

Claim 18 was rejected under 35 U.S.C. 102(e) as being anticipated by Lee. Claim 18 is copied below:

> A direct memory access controller, said direct memory access controller comprising:
> a state logic machine for receiving a single command to provide a specified range of a plurality of sequential data words, wherein the single command expressly states a starting address and an ending address of said specified range; and
> a memory controller for fetching a first portion of the specified selectable range and a second portion of the specified selectable range after fetching the first portion, wherein the second portion of the range has a lower address than the first portion, after the state logic receives the single command including the starting address and the ending address.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Assignee respectfully submits that the rejection to claim 18 is in error because each and every element as set forth in the claim are not found in Lee, either expressly or inherently.

A. THE REJECTION TO CLAIM 18 SHOULD BE REVERSED BECAUSE LEE DOES NOT TEACH A "*STATE MACHINE FOR RECEIVING A COMMAND*"

Examiner argues that the term "state logic machine" is unconventional, supporting the argument with a google search. It is unclear as to the exact term search, e.g., state logic machine, or "state logic machine". Appellant has similarly searched Google, using the search term "state logic machine", with the quotations. The result of the search shows usage of the term in a variety of sources, including U.S. Patents, University web pages, technical papers, and even a book on MOS digital electronics. The results of Appellant's search is provided in the evidence appendix.

Lee shows a DSCU 203a comprising a state machine 404. Appellant respectfully submits that the only portion of Lee that can possibly be considered the "state logic machine" is the "state machine 404". Thus it is indeed relevant and reasonable (contrary to Examiner's argument, Answer at 16) to require that the "state machine 404" specifically

receives the command to meet the limitation, "a state logic machine for receiving a single command".

Next Examiner extensively discusses the definition of "command", "instruction", and "opcode". However, the foregoing discussion does not change a very simple fact – without an opcode, or identification of an operation, there is no "command" or "instruction".

Examiner provides a definition of "command" as "A signal that initiates an operation defined by an instruction" from the American Heritage College Dictionary. While Examiner places great emphasis on "a signal", see Answer at 17, it is noted that the foregoing is not just "a signal", but one that "initiates an operation defined by an instruction". Note additionally, that the Microsoft Computer Dictionary cited by Examiner indicates that a "command" is, at the least, "an instruction". Additionally, according to the Computer Desktop Encyclopedia, a "command" is defined as an "Instruction for a computer". www. *computer.yourdictionary.com/***command***.*

Appellant respectfully submits that in the context of the present invention and the Lee reference, logic and microprocessor level electronics, the most appropriate definition of "command" is "an instruction". Appellant hereby offers to so define command on the record, and additionally, is willing to agree to amendment of "command" to "instruction".

Notwithstanding the foregoing, Examiner seeks to establish that an "opcode" and an "instruction"/"command" are different terms.

Ordinary skilled artisan understands that the plain meaning of opcode is only a portion of an instruction. An instruction may contain both opcode and operand. Thus, opcode is not a command or an instruction, and opcode has nothing to do with the claimed "single command".

The foregoing argument is misleading. The opcode is not just a portion of an instruction or command, it is an *essential* part of an instruction and command. For example, note that Examiner's quotation from Wikipedia actually provides Appellant's argument. See Answer at 15, n. 4 (quoting Wikipedia). The quote confirms that an instruction has an *opcode* and may or may not have *operands*. Note that the author of the statement was specific enough to note that an instruction may lack operands, but does not make the same statement about opcodes. This suggests that the omission of any statement that an instruction may lack an opcode was deliberate.

Thus, to say that "opcode has nothing to do with the claimed 'single command'" is in error.

Examiner then misinterprets the specification 0034 as "concord with Lee's signals and DSCU 203". The fact that "the command can be accompanied by a control signal indicating that the data words in the address range are to be provided to the MPEG video decoder 445 in the reverse order, e.g., 505(n), 505(n-1)...505(x)", Specification at 0034, demonstrates that the command and control signal are *different* entities.

Finally, Examiner reasons as follows:

> As appellant expressively indicates that Lee's arcs are conditions, examiner considers appellant agreeing Lee's arc represents command.
>
> Lee never mentions that the state transitions or the arcs are 'conditions'
>
> Examiner found no reason that a condition cannot be realized or interpreted as a command…

The foregoing reasoning is in error for several reasons. First, the mere fact that Lee "never mentions that the state transitions or the arcs are 'conditions'" does not change the fact that they are conditions. Additionally, as Examiner notes "Lee uses the terminology 'condition' 502/602". Moreover, Appellant submits that the difference between a "condition" and a "command" is entirely supported by dictionary definition, contrary to Answer at 17. Finally, interpretation of a condition at a command, because "Examiner found no reason" not to, is an error of law. The burden lies on Examiner to establish a reason to make the following construction.

Finally, in the Appeal Brief, Appellant showed that state diagrams can indeed change states without using commands, as in the example of flip-flops. Examiner refers to the foregoing example as "irrelevant", "oversimplified". It is noted that Figure 9 is a state diagram as opposed to a flow diagram. The state diagram merely distinguishes the different states from one another. Simple flip flops are often used to effectuate state diagrams with as few as ten states, such as shown in Figure 9.

Accordingly, Appellant respectfully requests that the rejection to claim 18 be <u>REVERSED</u>.

B.   THE REJECTION TO CLAIM 18 SHOULD BE REVERSED BECAUSE LEE DOES NOT TEACH A "SINGLE COMMAND TO *PROVIDE A SPECIFIED RANGE OF A PLURALITY OF SEQUENTIAL DATA WORDS"*

Answer at 18-19 appears to respond to Section VII.B. Appellant argued that Lee does not teach a "*single* command to provide a specified range of a plurality of sequential data words", as opposed to multiple commands. The Answer at 18-19 does not argue that Lee teaches "provid[ing] a specified range of a plurality of sequential data words" with a *single* command.

Accordingly, Appellant respectfully requests that the rejection to claim 18 be <u>REVERSED</u>.

C.   LEE DOES NOT TEACH "WHEREIN THE SINGLE COMMAND <u>EXPRESSLY</u> STATES A *STARTING ADDRESS* AND AN *ENDING ADDRESS"*

Examiner first notes that "The claim clause 'the single command expressly states a starting address and an ending address of said specified range are also results of claim amendment filed on December 11, 2009. Thus, in view of prosecution history, examiner considers appellant agrees the claim amendment made on December 11, 2009 would be necessary to overcome the cited Lee."

Appellant submits that the following conclusion is in error as there is no legal basis to conclude that the making of a claim amendment is a concession that any or all other limitations are met by the prior art. Moreover, Appellant submits that so concluding would discourage amendments to claims, increase the number of appeals, and increase the length of patent examinations.

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Finally, contrary to Examiner's argument that "the level of 'expressly state' is the level … explicitly in the specification which is found to be none", the foregoing limitation is amply supported in the specification. While Examiner observes that "At most, appellant discloses the starting address and ending address of a video packet". While the specification discloses that "The video packet 340 is received and decoded by the MPEG video decoder 445 starting from the word 505(x) storing the beginning of the video packet 340, and proceeding to the word 505(n) storing the end of the video packet 340" at 0025, the specification also includes:

> The MPEG video decoder 445 receives a video packet 340 by looking up the starting address and the ending address of a video packet 340 in the start code table 507. <u>The MPEG video decoder 445 can then command the DMA engine 510 to fetch the words 505(x)...505(n) that store the video packet 340</u>. Responsive thereto, the DMA engine 510 fetches and provides the words 505(x)...505(n) that store the video packet 340.

Specification at 0026. See also, Specification at 0034.

The foregoing clearly demonstrates a command to fetch from an express starting address, 505(x) and express ending address, words 505(n).

Accordingly, Appellant respectfully requests that the rejection to claim 18 be <u>REVERSED</u>.

D. LEE DOES NOT TEACH "FETCHING A FIRST PORTION OF THE SPECIFIED SELECTABLE RANGE AND A SECOND PORTION OF THE SPECIFIED SELECTABLE RANGE"

Appellant noted that "the range" takes antecedent basis from "a state logic machine for receiving a single

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command to provide a specified range of a plurality of sequential data words". Appeal Brief at 13.

The Final Office Action and Answer read the "state logic machine" onto DSCU, and the command onto 601. Lee does not teach buffer controller 1113 fetches any range specified in command 601 that is ever received by state machine 404, even if command 601 is deemed to teach a specified range, and state machine 404 is deemed to receive command 601.

On the one hand, Examiner reads "a state logic machine for receiving a single command to provide a specified range of a plurality of sequential data words" on DSCU 203a and command 601. On the other hand reads "first portion of the specified selectable *range* and a second portion of the specified selectable *range*" onto the data coming into barrel shifter 1104. It is noted that the barrel shifter 1104 is not the DSCU 203a, nor are the bits entering the barrel shifter specified by command 601. Thus, even if, for the sake of argument, the upper 32 bits and lower 32 bits are portions of selectable range, they are different from anything received at DSCU 203a and specified by command 601. Thus, Lee does not "first portion of the specified selectable range and a second portion of the specified selectable range".

The Answer at 21 mostly repeats the arguments made in the final office action and does not specifically address the foregoing.

Accordingly, Appellant respectfully requests that the rejection to claim 18 be REVERSED.

E. LEE DOES NOT TEACH "A SECOND PORTION OF THE SPECIFIED SELECTABLE RANGE AFTER FETCHING THE FIRST PORTION, WHEREIN THE SECOND PORTION OF THE RANGE HAS A LOWER ADDRESS THAN THE FIRST PORTION"

The Final Office Action and Answer indicate that the foregoing is taught at "col. 13, lines 27-35, barrel shifter 1104, the new fetch is always shift into lower 32 bit address".

Appellant argued that those of ordinary skill in the art would deem a "lower address" to be the address that the second portion is fetched *from*. Section VII.E. The Answer at 21 appears to address this limitation, but does not address this specific argument.

Accordingly, Appellant respectfully requests that the rejection to claim 18 be <u>REVERSED</u>.

F. DEPENDENT CLAIMS 19-23 AND 29

Additionally, claims 19-23, 29, and 30 depend on claim 18. Accordingly, Appellant respectfully requests reversal of these rejections, as well.

VIII. ARGUMENT: CLAIM 20

Claim 20 was rejected as anticipated by Lee. Claim 20 is dependent on claim 18. The limitations of claims 20 are copied below:

> 20. (Previously Presented) The direct memory access controller of claim 18, further comprising:
> a local buffer for storing the first and second portions in a forward address order, said local buffer comprising a plurality of data words.

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The Final Office Action at 9 indicates that "a local buffer" is taught at col. 6, line 58-60, "cache memory" and Fig. 16, DBC 203f. The foregoing is in error.

However, Lee does not teach that either element store "the first and second portions".

Even if, *arguendo*:

Lee teaches "a first portion (fig. 11, a portion of **VLD input buffer** 1112; col. 13 lines 27-35, fetch into barrel shift 1104 to lower 32 bit) of the specified selectable range and a second portion (fig. 11, a next portion of **VLD input buffer** 1112; col. 13, lines 27-35, move lower 32 bit to higher 32 and fetch new lower 32 bit)"

Lee does not teach the foregoing "first portion" and "second portion" would not be stored in either the DBC_MEM 203f or the RISC cache.

The Answer at 21-22 characterizes the foregoing argument as:

> Appellant argues that Lee does not teach 'a first and second portion of buffer with sole reason that Lee disclsoes a single VLD buffer (pages 14-15). Examiner respectfully disagrees with appellant, as appellant discloses a single buffer as well.

Appellant submits that the foregoing does not correctly characterize Appellant's argument and accordingly, does not adequately address it. Accordingly, Appellant reiterates the foregoing argument as the basis to request reversal of the rejection to claim 20.

IX. ARGUMENT: CLAIM 24

Claim 24 was rejected under 35 U.S.C. 102 as anticipated by Lee. Claim 24 is copied below:

> A method for fetching data words, said method comprising:
>
> receiving a single command to provide a range of a plurality of sequential data words in a memory, wherein the command expressly states a starting at a beginning address and ending at an ending address of said range;
>
> fetching a portion, in a forward address order, of the range of sequential data words, said wherein said portion of the range of sequential data words consists of a predetermined amount of data words that conclude with and precede the ending address, and wherein the predetermined amount of data words is equivalent to a capacity of a local buffer;
>
> storing the predetermined amount of data words that conclude with and precede the ending address in the local buffer;
>
> fetching, in the forward address order, at least one preceding portion of the range of sequential data words, wherein each of the preceding portions of the range of sequential data words consist of the predetermined amount of data words; and
>
> wherein a one of the preceding portions of the range of sequential data words comprises the starting address, truncating those data words that precede the beginning address.

Appellant respectfully incorporates the arguments in Section VII and requests that the rejection to claim 24 and dependent claims 25-28 be <u>REVERSED</u>.

Additionally, claim 24 recites, among other limitations, "wherein a one of the preceding portions of the range of sequential data words comprises the starting address, *truncating those data words that precede the beginning address*."

The Final Office Action indicates that the foregoing is taught at col. 10, lines 49-55, backward decoding; col. 15, lines 49-52, MPEG-4 rewinding and error resilience, the point of error has beginning address.

Appellant respectfully submits that the foregoing is in error. It is noted that "the starting address" takes antecedent basis to "wherein the command expressly states a starting at a beginning address and ending at an ending address of said range".

Lee does not teach that that the "wherein the command expressly states a starting at a beginning address" wherein "point of error" is the beginning address. Moreover, if the point of error is the beginning address, Lee does not teach truncating *prior* to the "point of error".

Accordingly, Lee does not teach "wherein a one of the preceding portions of <u>the</u> range of sequential data words comprises the starting address, *truncating those data words that precede the beginning address*."

Appellant has reviewed Examiner's Answer and cannot find any portion that addresses this argument. Examiner however does indicate that:

> At last, examiner perceives appellant's intention on seeking patent after a particular MPEG bit stream reversing approach with a revere signal to a multiplexer (mux) 555 as shown in figure 5, abstract and invention title. However, Lee discloses the same reversing approach with reversal section 1305 and reversible variable

length decoder RVLD 203bb as in figures 2 and 12. Moreover, appellant does not expressively claim such a structure as shown in figure 5, nor does appellant argue the claims for such a reverse signal operation. Therein examiner considers that appellant concedes on Lee disclosing the claimed bit reversal operations. The argued claim limitations are generically broad to any application as well as unspecific to the reversal bit order in appellant's invention endeavor.

First, Appellant's invention is defined by the claims, not Examiner's speculation of Appellant's intention. Furthermore, there is no legal basis to conclude that the failure to claim a specific structure or feature or argue a limitation in a patent application is a *concession* that the foregoing is taught in a particular prior art reference or even prior art.

Moreover, to examine the patent application based on speculation of intent would significantly reduce the objectiveness and introduce arbitrariness to the patent examination process. Requiring an Applicant to claim each and every feature and argue each and every limitation at the risk of making an admission of prior art, would significantly increase the cost and length of the examination process.

Finally, rejection of claim 24 or any other claim on the foregoing basis as anticipated under 35 U.S.C. 102 by the Lee reference would be contrary to well established law that "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Accordingly, Appellant requests that the rejection to claim 24 and dependent claims 25-27 be <u>REVERSED</u>.

X.   ARGUMENT: CLAIM 30

Claim 30 was rejected under 35 U.S.C. 102 as anticipated by Lee.   Appellant respectfully incorporates the arguments in Section VII and requests that the rejection to claim 30 be <u>REVERSED</u>.

XI.   CONCLUSION

For at least the foregoing reasons, the Board of Patent Appeals and Interferences is respectfully requested to <u>REVERSE</u> the rejections to claims 18-30. The Commissioner is hereby authorized to charge any fees for any action requested herein to deposit account 13-0017.

Dated: <u>April 4, 2011</u>   Respectfully submitted,

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CLAIMS APPENDIX

18. (Previously Presented) A direct memory access controller, said direct memory access controller comprising:

a state logic machine for receiving a single command to provide a specified range of a plurality of sequential data words, wherein the single command expressly states a starting address and an ending address of said specified range; and

a memory controller for fetching a first portion of the specified selectable range and a second portion of the specified selectable range after fetching the first portion, wherein the second portion of the range has a lower address than the first portion, after the state logic receives the single command including the starting address and the ending address.

19. (Previously Presented) The direct memory access controller of claim 18, wherein the memory controller fetches the first portion of the range and the second portion of the range in a forward address order.

20. (Previously Presented) The direct memory access controller of claim 18, further comprising:

a local buffer for storing the first and second portions in a forward address order, said local buffer comprising a plurality of data words.

21. (Previously Presented) The direct memory access controller of claim 20, wherein the plurality of data words

of the local buffer are narrower in width than the sequential data words.

22. (Previously Presented) The direct memory access controller of claim 20, further comprising:

a port for transmitting the contents of the plurality of data words of the local buffer in a reverse address order.

23. (Previously Presented) The direct memory access controller of claim 22, further comprising:

at least one multiplexer for reversing the bit positions of contents of at least one of the data words of the local buffer.

24. (Previously Presented) A method for fetching data words, said method comprising:

receiving a single command to provide a range of a plurality of sequential data words in a memory, wherein the command expressly states a starting at a beginning address and ending at an ending address of said range;

fetching a portion, in a forward address order, of the range of sequential data words, said wherein said portion of the range of sequential data words consists of a predetermined amount of data words that conclude with and precede the ending address, and wherein the predetermined amount of data words is equivalent to a capacity of a local buffer;

storing the predetermined amount of data words that conclude with and precede the ending address in the local buffer;

fetching, in the forward address order, at least one preceding portion of the range of sequential data words, wherein each of the preceding portions of the range of sequential data words consist of the predetermined amount of data words; and

wherein a one of the preceding portions of the range of sequential data words comprises the starting address, truncating those data words that precede the beginning address.

25. (Previously Presented) The method of claim 24, further comprising:

loading the portion and the at least one preceding portions of the sequential data words into the local buffer.

26. (Previously Presented) The method of claim 25, further comprising:

reversing the portion and the at least one preceding portions of the range of sequential data words.

27. (Previously Presented) The method of claim 26. further comprising:

reversing the truncated one of the preceding portions of the range of sequential data words that comprises the beginning address.

28. (Previously Presented) The direct memory access controller of claim 18, wherein the first portion and the second portion are adjacent to each other.

29. (Previously Presented) The direct memory access controller of claim 18, wherein the specified selectable range of the plurality of sequential data words is less than a memory storing the plurality of sequential data words.

30. (Previously Presented) A system for decoding video data, said system comprising:

a memory for storing a packetized elementary stream, said packetized element stream comprising a plurality of packets;

a start code table for storing starting addresses and ending addresses of said plurality of packets;

a video decoder for decoding a particular one of the plurality of packets, wherein the video decoder looks up the starting addresses and the ending addresses of the particular one of the plurality of packets and issues a single command to fetch the packet, wherein the single command expressly includes a starting address and an ending address associated with the particular one of the plurality packets; and

a direct memory access controller, said direct memory access controller comprising:

a state logic machine for receiving the single command; and

a memory controller for fetching a first portion of a range, said range comprising sequential data words from the starting address to the ending address for the particular one of the plurality of packets, and a second portion of the range after fetching the first portion, wherein the second portion of the range has a lower address than the first portion, after the state logic receives the

single command including the starting address and the ending address.

EVIDENCE APPENDIX

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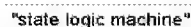
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Claims - Patents
Apparatus as set forth in claim 10 wherein the combinational logic portion of said sequential
state logic machine comprises a read-only memory means ...
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All Optical Digital Logic: Full Addition or Subtraction on a Three ...
By encoding the digits to be operated on as 'on' or 'off' laser input signals we show how STIRAP
can be used to implement a finite **state logic machine**. ...
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Logic operations in a doped solid driven by stimulated Raman ...
by P Roos - 2011
Mar 29, 2011 ... flip-flop, i.e., a basic finite **state logic machine**. If we restrict the gate to two
subsequent input bits (i.e., two SP pairs), we ...
link.aps.org/doi/10.1103/PhysRevA.83.030421

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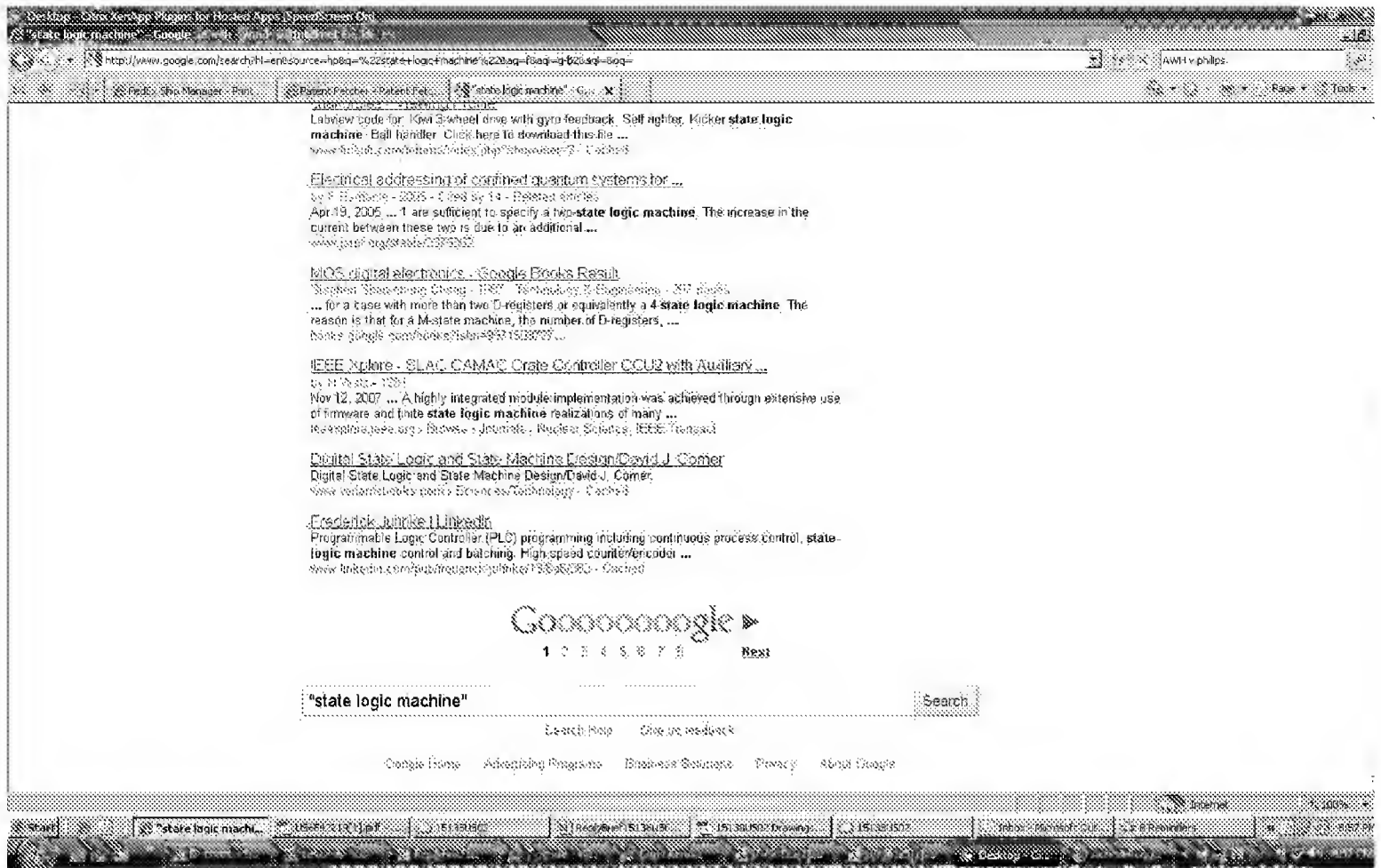www.pnas.org/stable/03752802

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